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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,460	01/27/2004	Davide Chiola	IR-2536 (2-3568)	3182
2352	7590	11/02/2004	EXAMINER	
OSTROLENK FABER GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NY 100368403			DANG, TRUNG Q	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/766,460	CHIOLA, DAVIDE	
	<b>Examiner</b>	<b>Art Unit</b>	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 August 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. ____   |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____  | 6) <input type="checkbox"/> Other: ____                                     |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 9-10, 12-18, and 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Temple (US 4,941,026).

With reference to Fig. 4 taken in conjunction with Fig. 2A for the purpose of better understanding the rejection, Temple teaches a trenched Schottky diode device comprising:

a semiconductive substrate 12a of a first conductivity type and a first concentration (N+) of dopants (Fig. 2A);

a semiconductive layer 12 of said first conductivity type and a second concentration (N) of dopants, said first concentration of dopants being higher than said second concentration of dopants (Fig. 4);

a plurality of trenches 24 extending to a depth inside said semiconductive layer, each of said trenches including opposing sidewalls and a bottom, and each being adjacent at least one mesa (Fig. 4 and col.11, lines 58-63);

a first insulation layer 36 of a first thickness on each sidewall of each of said

trenches (Fig. 2A);

a second insulation layer 38 of a second thickness on said bottom of each of said trenches, said second thickness being greater than said first thickness (Fig. 2A and col.13, lines 35-47);

a schottky barrier in schottky contact with said mesas (col. 21, lines 48-52);

a first electrical contact 23 (Fig. 4) in contact with said schottky barrier; and

a second electrical contact 11 (Fig. 2A) in electrical contact with said semiconductive substrate.

Note that the schottky barrier is a depletion region created at the interface of the metal 23 and the semiconductor substrate, and metal 23 is in contact with the depletion layer or the schottky barrier.

For claims 3 and 4, Fig. 4 shows conductive polysilicon electrodes 40 disposed in each trench. For the limitation regarding the first contact being electrically connected to the polysilicon electrodes, see col. 18, lines 21-24 for the teaching that metallization layer is formed to interconnect the regions of a plurality of device cells. Note that the metallization layer connects the first contact with the polysilicon electrode in a trench Schottky diode device.

For claims 5-6, see col. 8, lines 14-24 and col. 17, line 34.

For claims 9-10, see the table in col. 14.

For claim 12, it is noted that the method of which the first or the second oxide

layer is formed carries no patentable weight in a device claim since it is well settled that the patentability of a product does not depend on its method of production.

In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

For the method claims, Temple teaches a method for manufacturing a  
trenched schottky diode comprising:

providing a semiconductive body 12 (Fig.4);

forming a plurality of trenches 24 in said semiconductive body, each trench  
having opposing sidewalls, and a bottom, and each being adjacent a mesa;

covering said sidewalls of said trenches with an oxidation preventing  
layer of silicon nitride;

forming an oxide layer at the bottom of each of said trenches (col. 12, lines 46-  
64); and

forming a schottky barrier layer in schottky contact with each of said  
mesas (col. 21, lines 48-52).

For claims 14 and 18, see col. 12, lines 41-45 for the teaching of forming an  
oxide layer (oxide layer 36 in Fig. 2A) prior to forming the silicon nitride oxidation  
preventing layer.

For claims 16 and 17, see col.17, lines 37-64 for the teaching of etching the  
trench using a trench mask comprises a silicon nitride layer.

3. Claims 1-8 and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hijzen et al. (US 6,441,454).

With reference to Fig. 3, Hijzen teaches a trench Schottky diode device comprising:

- a semiconductive substrate 60 of a first conductivity type and a first concentration (N+) of dopants;
- a semiconductive layer 4a of said first conductivity type and a second concentration (N or N-) of dopants, said first concentration of dopants being higher than said second concentration of dopants;
- a plurality of trenches extending to a depth inside said semiconductive layer, each of said trenches including opposing sidewalls and a bottom, and each being adjacent at least one mesa;
- a first insulation layer 21x of a first thickness on each sidewall of each of said trenches;
- a second insulation layer 21y of a second thickness on said bottom of each of said trenches, said second thickness being greater than said first thickness;
- a schottky barrier 43 in schottky contact with said mesas;
- a first electrical contact 3 in contact with said schottky barrier; and
- a second electrical contact 34 in electrical contact with said semiconductive substrate.

For claims 2 and 12, it is noted that the method of which the first or the second oxide layer is formed carries no patentable weight in a device claim since it is well settled that the patentability of a product does not depend on its method of production. In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

For claims 3 and 4, see conductive polysilicon 31 disposed in each trench and electrically connected to the first electrical contact 3.

For the limitations of claims 5, 6, and 11, see col. 4, lines 6-28.

For claims 7 and 8, although the perimeter trench 18 (corresponding to the claimed termination trench) of the embodiment depicted Fig. 3 does not have an outer sidewall, Hijzen discloses that alternative features shown in one embodiment may be adopted in another embodiment (col. 5, lines 18-23). Thus, the embodiment of Fig. 1 having the perimeter trench 18 bounded by inner and outer sidewalls includes the feature regarding thin oxide layer 21x and thick oxide layer 21y of the Fig. 3 embodiment.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 9-10 and 13-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hijzen et al. in view of Temple, both cited above.

With reference to Fig. 3, Hijzen teaches a trench Schottky diode device comprising:

providing semiconductive substrate 60 of a first conductivity type and a first concentration (N+) of dopants;

forming an epitaxial semiconductive layer 4a of said first conductivity type and a second concentration (N or N-) of dopants, said first concentration of dopants being higher than said second concentration of dopants;

forming a plurality of trenches extending to a depth inside said semiconductive layer, each of said trenches including opposing sidewalls and a bottom, and each being adjacent at least one mesa;

forming a first insulation layer 21x of a first thickness on each sidewall of each of said trenches;

forming a second insulation layer 21y of a second thickness on said bottom of each of said trenches, said second thickness being greater than said first thickness;

forming a schottky barrier 43 in schottky contact with said mesas;

forming a first electrical contact 3 in contact with said schottky barrier; and

forming a second electrical contact 34 in electrical contact with said semiconductive substrate.



Hijzen differs from the claims in the step of forming an oxidation preventing layer covering sidewalls of the trenches. Temple teaches a method for forming a trenched Schottky diode in which a gate oxide layer, which is thin at the sidewalls and thick at the bottom of the trench, is formed by covering the sidewalls of the trench with a nitride layer (corresponding to the claimed oxidation preventing layer) while exposing the bottom of the trench and then forming the thick oxide layer at said bottom (col. 12, lines 46-64). It would have been obvious to one of ordinary skill in the art to modify Hijzen's teaching by forming the thin oxide layer 21x and the thick oxide layer 21y utilizing the Temple's technique as described above because such method of forming gate oxide with varying thickness is known in the art, and the employment of a known process to make the same would have been within the level of one skilled in the art.

For claims 14 and 18, see col. 12, lines 41-45 in Temple for the teaching of forming an oxide layer (oxide layer 36 in Fig. 2A) prior to forming the silicon nitride oxidation preventing layer.

For claims 16 and 17, see col. 17, lines 37-64 in Temple for the teaching of etching the trench using a trench mask comprises a silicon nitride layer.

For claims 19 and 20, see Hijzen, Figs. 3 and 5, wherein trench mask 50 of silicon nitride, which is rendered obvious in light of Temple's teaching as noted above, is used to etch both inner trench 11 and perimeter trench 18.

For device claims 9-10, Hijzen's device described above taken with Temple's teaching disclosed in the table in col. 14 would render the claims obvious because such numerical values associated with the thickness of oxide layer 21x and 21y are desirable to ensure high voltage breakdown of the device as taught by Temple (col. 14, lines 27-31).

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 16-18 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites a limitation "an oxidation preventing layer" that is also recited in the base claim 13, which renders claim 16 and its dependent claims confusing. For example, each of claims 17, 18, and 20 makes reference to the oxidation preventing layer, and one cannot tell whether the claims refer to the oxidation preventing layer of claim 13 or the oxidation preventing layer of claim 16. Clarification is required.


8. Any inquiry concerning this communication or earlier communications from

the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang  
Primary Examiner  
Art Unit 2823



10/29/04